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EXAMINER	
CRUTCHFIELD, CHRISTOPHER M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,613	HALL ET AL.	
	Examiner	Art Unit	
	Christopher Crutchfield	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 11** recites the limitation "said plurality". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-4, 10, 12-15, 31, and 34** are rejected under 35 U.S.C. 102(e) as being anticipated by *Uzun*, et al. (US Patent No. 6,961,342 B1).

Regarding claim 1, *Uzun* discloses a packet switch:

a. Having plural input sectors (Fig. 4, Elements 410a-c) and output sectors, (Fig. 4, Elements 420a-c) each input sector being arranged to hold at least one queue per output sector, (Fig. 5, IVOQ 0 to K-1) each output sector having plural output ports (Fig. 4, Element 470) and being arranged to hold at least one queue per output port (Fig. 4, Element 422). (The system of *Uzun* discloses a switch that utilizes multiple input sectors connected to multiple output sectors via several parallel links and a central switch fabric [Fig. 4 and Column 12, Lines 44-64]. The input sectors each contain multiple virtual output queues into which the data received from each input in the sector is placed [Fig. 4 and Column 12, Lines 44-64]. The Output Queues may be arranged in one of two ways. First, a shared virtual output queue may be created for each output port of each output group [i.e. all output ports] [Fig. 5 and Column 13, Lines 7-16]. Second, to simplify scheduling by reducing the number of VOQ's and to enhance multicasting, a single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50]. Turning to the output sectors, each output sector may likewise hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

b. Wherein the input sectors are connected to the output sectors via links configured to afford speed-up of data transfer, wherein the links comprise a set of links (Fig. 4, Elements 0 to M-1 and Column 9, Line 37, Column 15, Lines 15-17, Column 19, Lines 9-32, Column 32, Lines 32-38). (The system of *Uzun* discloses that each input sector comprises a number of links to the output sector, [Fig. 4, Element 440] and that speedup may be implemented Such that the bandwidth out of the Input Shared Block Exceeds the

bandwidth of the individual inputs [Fig. 4, Elements 0 to M-1 and Column 9, Line 37, Column 15, Lines 15-17, Column 19, Lines 9-32, Column 32, Lines 32-38].)

c. Wherein the switch has means for cyclically connecting different subsets of the set of links between the input sectors and the output sectors, and means responsive to statistical variations in traffic applied to input ports of said input sectors to vary the set of links (Column 14, Line 57 to Column 15, Line 5). (The system of *Uzun* implements Round Robin connection of each Virtual Output Group. This results in the cyclic connection of each VOQ to the corresponding Output Shared block. The round robin scheduling is capable of altering the cyclic pattern to allow an Output Group to transmit twice if another output group is idle [Column 14, Line 57 to Column 15, Line 5]. Round robin scheduling can be applied on a per group VOQ basis or a per output VOQ basis, depending on the type of output queuing in use [Column 14, Line 5 to Column 15, Line 5].)

Regarding claim 2, *Uzun* discloses a packet switch wherein each input sector is arranged to hold one queue per output of the output sectors to provide virtual output queuing (VOQ) (Fig. 5 and Column 13, Lines 7-16). (A shared virtual output queue may be created for each output port of each output group [i.e. all output ports] [Fig. 5 and Column 13, Lines 7-16] [See also Claim 1, Supra].)

Regarding claim 3, *Uzun* discloses a packet switch wherein each input sector is arranged to hold only one queue per output sector (Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50). (A single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50] [See also Claim 1, Supra].)

Regarding claim 4, *Uzun* discloses a packet switch having:

a. Plural input sectors (Fig. 4, elements 410a-c) and output sectors (Fig. 4, Elements 420a-c).

b. Each input sector having an input sector memory (Fig. 5, Element 412) and plural input ports, (Fig. 5, Elements jM to jM+M-1) each port being arranged to receive packet data, the input sector memory being arranged to store plural input queues of packet data from said input ports, at least one said input queue corresponding to each respective output sector, the input sector memory having a respective output for each said input queue (Fig. 5, elements Jm to Jm+M-1). (The system of *Uzun* discloses a switch that utilizes multiple input sectors connected to multiple output sectors via several parallel links and a central switch fabric [Fig. 4 and Column 12, Lines 44-64]. The input sectors each contain multiple virtual output queues into which the data received from each input in the sector is placed [Fig. 4 and Column 12, Lines 44-64]. The Output Queues may be arranged in one of two ways. First, a shared virtual output queue may be created for each output port of each output group [i.e. all output ports] [Fig. 5 and Column 13, Lines 7-16]. Second, to simplify scheduling by reducing the number of VOQ's and to enhance multicasting, a single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50].)

c. Each output sector having an output sector memory and plural output ports, the output sector memory being arranged to store plural output queues and having plural inputs for packet data and being arranged to pass packet data to a respective output port (Fig. 4,

Element 422 and 470 and Column 12, Lines 44-64). (The output sectors of *Uzun* may hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

d. The packet switch further having a population of links (Fig. 4. Element 440) and a control device (Column 19, Lines 9-32).

e. Wherein said population comprises plural links for carrying packet data between outputs of the input sector memory and inputs of the output sector memory (Fig. 4. Element 440 - See Also (b), Supra).

f. Wherein the control device is operable to form a selection of links from said population to provide speed-up, and thereby enable packet data transfer between said outputs and inputs using said selection of links and the control device being further operable to vary said selection to cope with changing traffic conditions (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38). (The system of *Uzun* may implement multiple round robin queuing. In such a queuing architecture, a single GVOQ queue may be allocated multiple transmission links in order to provide a link speedup to handle excessive traffic bound for a particular GVOQ [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. The extra link may come from robbing another GVOQ of the opportunity to transmit, or from an extra link provided by an internal speedup in the switch [Column 32, Lines 34-38].)

Regarding claim 10, *Uzun* discloses a packet switch wherein each link has a similar packet rate to the line rate of packet flow at switch input ports (Column 9, Lines 27-40 and Fig. 4). (Each module/sector has the same number of inputs and outputs [Column 9, Lines 27-40 and Fig.]. Furthermore, the central switch operates with out speedup [i.e. at the combined line rate of all the inputs] and all the module output links operate at the same speed [Column 13, Lines 42-47]. Therefore, the sum of the bandwidth of the module output links equals the control switch bandwidth which equals the sum of the bandwidths of the input ports. Since the number of input ports and module output links are the same, their bandwidth must likewise be equal as well.)

Regarding claim 12, *Uzun* discloses a method of routing packets in a packet switch having plural input sectors and output sectors, each input sector being arranged to hold at least one queue per output sector, each output sector having plural output ports and being arranged to hold at least one queue per output port (Figs. 4 and 5 - See Claim 4, Supra) the method comprising:

a. Providing a set of links for connecting each input sector queue to respective output sector queues (Fig. 4, Element 440). (The system of *Uzun* discloses a switch that utilizes multiple input sectors connected to multiple output sectors via several parallel links and a central switch fabric [Fig. 4 and Column 12, Lines 44-64]. The input sectors each contain multiple virtual output queues into which the data received from each input in the sector is placed [Fig. 4 and Column 12, Lines 44-64]. Each per to VOQs is connected to the central switch and the outputs by multiple parallel links [Fig. 4, Element 440]. The Output Queues may be arranged in one of two ways. First, a shared virtual output queue may be created for each output port of each output group [i.e. all output ports] [Fig. 5

and Column 13, Lines 7-16]. Second, to simplify scheduling by reducing the number of VOQ's and to enhance multicasting, a single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50]. Turning to the output sectors, each output sector may likewise hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

b. Connecting at least some input sector queues to respective output sector queues using a subset of said set of links, said subset affording speed-up of data transfer, and cyclically selecting different subsets of the set of links between the input sectors and the output sectors (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38). (The system of *Uzun* may implement multiple round robin queuing in order to cycle through each subset of links between the different sectors. As long as each VOQ of each sector has data for the appropriate output and does not exceed a danger threshold, the round robin scheduler cyclically transmits the data [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. However, if a VOQ exceeds a predefined threshold, the scheduler will respond by allocating multiple transmission links in order to provide a link speedup to handle excessive traffic bound for a particular GVOQ [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. The extra link may come from robbing another GVOQ of the opportunity to transmit, or from an extra ink provided by an internal speedup in the switch [Column 32, Lines 34-38].)

Regarding claim 13, *Uzun* discloses a method further comprising determining statistical variations in traffic applied to input ports of said input sectors and in response thereto vary the

set of links (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38). (The system of *Uzun* may implement multiple round robin queuing in order to cycle through each subset of links between the different sectors. As long as each VOQ of each sector has data for the appropriate output and does not exceed a danger threshold, the round robin scheduler cyclically transmits the data [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. However, if a VOQ exceeds a predefined threshold, the scheduler will respond to the changing traffic conditions by allocating multiple transmission links in order to provide a link speedup to handle excessive traffic bound for a particular GVOQ [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. The extra link may come from robbing another GVOQ of the opportunity to transmit, or from an extra ink provided by an internal speedup in the switch [Column 32, Lines 34-38].)

Regarding claim 14, *Uzun* discloses a method wherein the determining step comprises monitoring input queue states (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38 – See Claim 13, Supra).

Regarding claim 15, *Uzun* discloses a method wherein the determining step comprises wherein the determining step comprises monitoring input packet arrivals (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38). (The system of *Uzun* discloses monitoring the state of each virtual output queue. Whenever a packet arrives it is added to the appropriate VOQ. Therefore monitoring the VOQ monitors input packet arrivals.)

Regarding claim 31, *Uzun* discloses a method of routing packet traffic using a device having a number of input ports and said number of output ports, the method comprising:

a. Applying packet traffic at said input ports, deserialising signals at each input port to provide first intermediate signals, said first intermediate signals being disposed in a

group of said number of signals associated with each input port, whereby said number of groups is formed (Fig. 4, Element 430). (The system of *Uzun* discloses that the signals received from each input port are desterilized into a set of first intermediate signals, wherein one of each signals is associated with a VOQ for the group of inputs [Column 12, Lines 44-65]. The intermediate signal is then sent to the appropriate VOQ, where it is multiplexed with the intermediate signals for the other inputs at the input to the VOQ to form a second intermediate signal which is stored in the VOQ [Fig. 5, VOQs and Column 12, Lines 44-65])

b. Transposing said first intermediate signals among said groups to provide transposed groups containing one first intermediate signal from each said group and multiplexing together the transposed groups of first intermediate signals, to provide said number of second intermediate signals (Fig. 5, VOQs and Column 12, Lines 44-65 - See (a), Supra).

c. Distributing said second intermediate signals among said number of queue storage locations according to the output port of the second intermediate signal (Fig. 5, VOQs and Column 12, Lines 44-65 - See (a), Supra).

d. Selecting data from said storage locations and serially outputting data from locations for sequential output ports (Column 13, Lines 6-50). (The scheduler of *Uzun* schedules each VOQ in a FIFO Round Robin Order. Therefore, the VOQs are sent in order from smallest to largest to the corresponding output ports, from smallest to largest. The

transmission of a single VOQ occurs on a single transmission line and is serial [Column 12, Lines 44-65].)

e. Deserialising said serially output data to provide third intermediate signals, said third intermediate signals being disposed in a group of said number of signals, whereby said number of groups is formed (Fig. 4 and Column 12, Lines 44-64 and Column 13, Lines 51-65). (At the output, the system of *Uzun* takes the Shared output block queues and de-serializes the data and then transmits the data to the appropriate output for parallel output [Fig. 4 and Column 12, Lines 44-64 and Column13, Lines 51-65]).

f. Transposing said third intermediate signals among said groups to provide transposed groups containing one third intermediate signal from each said group and multiplexing together the transposed groups of third intermediate signals, to provide said number of output signals at said output ports (Fig. 4 and Column 12, Lines 44-64 and Column13, Lines 51-65 - See (e), Supra)

Regarding claim 34, *Uzun* discloses a method wherein each link has a similar packet rate to the line rate of packet flow at switch input ports (Column 9, Lines 27-40 and Fig. 4). (Each module/sector has the same number of inputs and outputs [Column 9, Lines 27-40 and Fig.]. Furthermore, the central switch operates with out speedup [i.e. at the combined line rate of all the inputs] and all the module output links operate at the same speed [Column 13, Lines 42-47]. Therefore, the sum of the bandwidth of the module output links equals the control switch

bandwidth which equals the sum of the bandwidths of the input ports. Since the number of input ports and module output links are the same, their bandwidth must likewise be equal as well.)

5. **Claims 17-18** are rejected under 35 U.S.C. 102(e) as being anticipated by *Miles*, et al (US Patent No. 6,665,495 B1).

Regarding claim 17, *Miles* discloses a line card interface device having plural optical paths between a first set of ports and a second set of ports, each optical path having a controllable shutter operable to enable or disable its path, the device further having means for selecting a set of said optical paths and means for cyclically connecting different subsets of the set of paths between the first and second set of ports (Column 9, Lines 34-57 and Fig. 4). (The system of *Miles* discloses a number of ingress edge units [i.e. Line Card Interfaces] that are connected to the egress edge units by a plurality of DWDM super packet links. The core switch module is made up of a plurality of paths that can connect any input DWDM super packet link to any output DWDM super packet link [Fig. 6]. The switch operates by closing all paths for a particular input DWDM super packet line except one, the desired DWDM super packet output link [Fig. 6 and Column 9, Lines 34-57]. The opening and closing of the paths is done cyclically according to a schedule that may be varied in response to changing traffic demands [Column 31, Lines 47-67 and Column 33, Lines 10-62].)

Regarding claim 18, *Miles* discloses a line card interface having means responsive to statistical variations in traffic flow to the line cards for varying the set of optical paths (Column 31, Lines 47-67 and Column 33, Lines 10-62).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claims 5-9 and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) as applied to claims 4 and 31 and further in view of *Krishna*, et al. (US Pre Grant Publication No. 2001/0050916 A1).

Regarding claim 5, *Uzun* discloses a packet switch wherein each input sector memory is arranged to store one input queue for each output port of the switch (Fig. 4, Element 422 and 470 and Column 12, Lines 44-64). (The output sectors of *Uzun* may hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

Uzun fails to disclose a packet switch wherein each input sector memory is arranged to store one input queue per input port of the sector for each output port of the switch. In the same field of endeavor, *Krishna* discloses a packet switch wherein each input sector memory is arranged to store one input queue per input port of the sector for each output port of the switch (Fig. 17 and Paragraphs 0117 and 0119). (The system of *Krishna* discloses input ports that use a separate VOQ for each output port [Fig. 17 and Paragraphs 0117 and 0119] and output ports that use separate queues for each input port.)

Therefore, since *Krishna* discloses the use of separate output ports for each input port, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the per-input port VOQ's of *Krishna* into the switch of *Uzun*. The per-input port VOQs of *Krishna* can be combined with the switch of *Uzun* by implementing a separate per output VOQs for each input port in the switch, as taught by *Krishna* and separately assigning links to each of the VOQs as taught by *Uzun* and *Krishna*. The motive to combine is to promote fairness among inputs in the same sector, by allowing each input to separately contend for access to the selection of links.

Regarding claim 6, *Uzun* discloses a packet switch wherein each output sector memory is arranged to store one output queue per output port of the sector (Fig. 4, Element 422 and 470 and Column 12, Lines 44-64). (The output sectors of *Uzun* may hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

Uzun fails to disclose a packet switch wherein each output sector memory is arranged to store one output queue per output port of the sector for each input port of the switch. In the same field of endeavor, *Krishna* discloses a packet switch wherein each output sector memory is arranged to store one output queue per output port of the sector for each input port of the switch (Fig. 17 and Paragraphs 0117 and 0119). (The system of *Krishna* discloses input ports that use a separate VOQ for each output port [Fig. 17 and Paragraphs 0117 and 0119] and output ports that use separate queues for each input port.)

Therefore, since *Krishna* discloses the use of a separate output queue for each input port, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the separate output queues of *Krishna* into the system of *Uzun* by keeping an output queue for each input at each output. The motive to combine is provided by *Krishna* and is to prevent blocking caused by simultaneous attempts to write to each output (Paragraphs 0117 an 0119).

Regarding claim 7, *Uzun* discloses a packet switch as wherein each input sector memory is arranged to store a single output queue per output sector (Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50). (A single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50] [See also Claim 1, Supra].)

Uzun fails to disclose a packet switch wherein each input sector memory is arranged to store a single output queue per output sector for each input port of the switch. In the same field of endeavor, *Krishna* discloses a packet switch wherein each input sector memory is arranged to store a single output queue per output sector for each input port of the switch (Fig. 17 and Paragraphs 0117 and 0119). (The system of *Krishna* discloses a system where each input maintains its own VOQs. The separated VOQs allow each input to separately contend for

access to the core switch/selection of links, thereby promoting fair bandwidth allocation among the links [Paragraphs 0071-0077].)

Therefore, since *Krishna* discloses the use of separate input VOQs to promote fair bandwidth allocation among input links, it would have been obvious to a person of ordinary skill in the at the time of the invention to split the per sector VOQs of the input sector if *Uzun* into separate links that may contend for access to each output link separately because the technique of splitting inputs in to separate input queues to promote fairness among the inputs during scheduling contention was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

Regarding claim 8, *Uzun* discloses a packet switch as wherein each output sector memory is arranged to store a single output queue per output port of the sector (Fig. 4, Element 422 and 470 and Column 12, Lines 44-64). (The output sectors of *Uzun* may hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64].)

Regarding claim 9, *Uzun* fails to disclose a packet switch wherein each link has a higher packet rate than the line rate of packet flow at switch input ports to provide said speed-up. In the same field of endeavor, *Krishna* discloses a packet switch wherein each link has a higher packet rate than the line rate of packet flow at switch input ports to provide said speed-up (Paragraph 0026).

Therefore, since *Uzun* discloses the use of a link speedup, it would have been obvious to implement the link speedup of *Krishna* into the teachings of *Uzun* by increasing the speed of each link in the central switch fabric to exceed the input line rate. The motive to combine is provided by *Krishna* and is to offer a switch fabric that more closely approximates the desirable properties of an output queued switch, where all inputs may transmit to a single output simultaneously (Paragraphs 0016-0020].

Regarding claim 33, *Uzun* fails to disclose a method wherein each link has a higher packet rate than the line rate of packet flow at switch input ports to provide said speed-up. In the same field of endeavor, *Krishna* discloses a packet switch wherein each link has a higher packet rate than the line rate of packet flow at switch input ports to provide said speed-up (Paragraph 0026).

Therefore, since *Uzun* discloses the use of a link speedup, it would have been obvious to implement the link speedup of *Krishna* into the teachings of *Uzun* by increasing the speed of each link in the central switch fabric to exceed the input line rate. The motive to combine is provided by *Krishna* and is to offer a switch fabric that more closely approximates the desirable properties of an output queued switch, where all inputs may transmit to a single output simultaneously (Paragraphs 0016-0020].

10. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) as applied to claim 4 and further in view of *Reeve*, et al. (US Pre Grant Publication No. 2002/0027902 A1)

Regarding claim 11, *Uzun* discloses a packet switch which comprises multiple input and output sectors wherein the input sectors contain individual virtual output queues.

Uzun fails to fails to disclose a packet switch wherein the control device comprises a processor constructed and arranged to construct a service matrix having integer entries in units of the link rate and having row and column sums equal to said plurality such that in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said matrix having elements formed by the said desired offered load at the switch inputs on the basis of each input and output port; and to decompose the service matrix into its

constituent permutations thereby to control said links using said permutations. In the same field of endeavor, *Reeve* discloses a packet switch wherein the control device comprises a processor constructed and arranged to construct a service matrix having integer entries in units of the link rate and having row and column sums equal to said plurality such that in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said matrix having elements formed by the said desired offered load at the switch inputs on the basis of each input and output port; and to decompose the service matrix into its constituent permutations thereby to control said links using said permutations (Paragraphs 0012-0021 and 0061-0095 and Figs 1, 3, and 4). (The system of *Reeve* discloses a system which maintains separate VOQ's at each ingress port [Fig. 1, Element 102]. The system of *Reeve* further discloses that the system schedules packet transmission by creating a desired load matrix/rate matrix [Paragraphs 0040 and 0074]. The rate matrix is then de-composed into a series of service matrices/configuration matrices which have rows and columns that add up to the total bandwidth on the links [Paragraphs 0060 to 0061]. The values contained in each rate matrix are integer values of 0 and 1 and are in units of the link rate, each corresponding to the transmission of a packet at the internal link rate. The system then implements the permutations to achieve the desire bandwidth allocation [Paragraphs 0073-0095].)

Therefore, since *Reeve* discloses the use of per port VOQs and the use of a service matrix, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the VOQs and Service Matrices of *Reeve* into the teachings of *Uzun*. The VOQs and Service Matrices of *Reeve* can be combined with the system of *Uzun* by implementing a separate VOQ for each input at each input sector to promote fairness among the input queues and to then schedule among the inputs and outputs using the rate matrix and service matrices as taught by *Reeve*. The motive to combine is to utilize separate queues at

each input to promote fairness and to utilize a simple matrix decomposition scheduling algorithm capable of operating at high speed.

11. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) as applied to claim 12 and further in view of *Reeve*, et al. (US Pre Grant Publication No. 2002/00272092 A1) and *Miles*, et al. (US Patent No. 6,665,495 B1).

Regarding claim 16, *Uzun* discloses a packet switch that treats each input sector and output sector as a separate port, but can utilize over speed to allow multiple simultaneous transmissions from a single output sector (Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38). (The system of *Uzun* discloses a switch that utilizes multiple input sectors connected to multiple output sectors via several parallel links and a central switch fabric [Fig. 4 and Column 12, Lines 44-64]. The input sectors each contain multiple virtual output queues into which the data received from each input in the sector is placed [Fig. 4 and Column 12, Lines 44-64]. Each ser to VOQs is connected to the central switch and the outputs by multiple parallel links [Fig. 4, Elelement 440]. The Output Queues may contain a single VOQ for each output sector may be utilized [Fig. 5 and Column 8, Lines 47-67 and Column 13, Lines 17-50]. Turning to the output sectors, each output sector may likewise hold a single output queue for each output port [Fig. 4, Element 422 and 470 and Column 12, Lines 44-64]. The system of *Uzun* may implement multiple round robin queuing in order to cycle through each subset of links between the different sectors. As long as each VOQ of each sector has data for the appropriate output and does not exceed a danger threshold, the round robin scheduler cyclically transmits the data [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. However, if a VOQ exceeds a predefined threshold, the scheduler will respond by allocating

multiple transmission links in order to provide a link speedup to handle excessive traffic bound for a particular GVOQ [Column 19, Lines 9-32 and Column 30, Lines 34-52 and Column 32, Lines 34-38]. The extra link may come from robbing another GVOQ of the opportunity to transmit, or from an extra ink provided by an internal speedup in the switch [Column 32, Lines 34-38].)

Uzun fails to disclose a method wherein the providing step comprises constructing a service matrix having integer entries in units of the internal link rate and having row and column sums equal to said plurality such that, in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said desired traffic matrix having elements formed by the said desired offered load at the switch input ports on the basis of each input port and output port and decomposing the service matrix into its constituent permutations and controlling said links using said permutations. In the same field of endeavor, *Reeve* discloses a method wherein the providing step comprises constructing a service matrix having integer entries in units of the internal link rate and having row and column sums equal to said plurality such that, in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said desired traffic matrix having elements formed by the said desired offered load at the switch input ports on the basis of each input port and output port and decomposing the service matrix into its constituent permutations and controlling said links using said permutations (Paragraphs 0012-0021 and 0061-0095 and Figs 1, 3, and 4). (The system of *Reeve* discloses a system which maintains separate VOQ's at each ingress port [Fig. 1, Element 102]. The system of *Reeve* further discloses that the system schedules packet transmission by creating a desired load matrix/rate matrix [Paragraphs 0040 and 0074]. The rate matrix is then de-composed into a series of service matrices/configuration matrices which have rows and columns that add up to the total bandwidth on the links

[Paragraphs 0060 to 0061]. The values contained in each rate matrix are integer values of 0 and 1 and are in units of the link rate, each corresponding to the transmission of a packet at the internal link rate. The system then implements the permutations to achieve the desire bandwidth allocation [Paragraphs 0073-0095].)

Therefore, since *Reeve* discloses scheduling between inputs and outputs using a deconstructed matrices, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the matrix deconstruction of *Reeve* into the teachings of *Uzun*. The matrix deconstruction of *Reeve* can be combined with the system of *Uzun* by treating each output sector as a single output, as taught by *Uzun* and implementing matrix decomposition to determine the interconnection of the input and output queues, as taught by *Reeves*, but setting the maximum ingress forwarding rate to the total available link bandwidth (which exceeds 1.0 as stated in *Reeves* because the system of *Uzun* employs a speedup), as taught by *Reeves* and then decomposing the Rate Matrix into the corresponding Traffic Matrices. The motive to combine is to allow for simple scheduling using rate decomposition.

Uzun and *Reeve* fail to disclose that the deconstructed matrices are used cyclically. In the same field of endeavor, *Miles* discloses using a series of deconstructed matrices cyclically (Column 31, Lines 47-67 and Column 33, Lines 10-60). (The system of *Miles* discloses periodically establishing a set of decomposed cyclic matrices that determine the relative bandwidth allocations for each port [Column 31, Lines 47-67 and Column 33, Lines 10-60].) Therefore, since miles discloses the periodic use of a set of configuration matrices, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the cyclic configuration matrices of *Miles* into the system of *Uzun* by cyclically repeating the configuration matrices from one period of the system over multiple periods. The motive to combine is to reduce processing power by re-using the configuration matrices.

12. **Claims 19, 20, 21, 22, 23, 24, 25, 26, 27 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) in view of *Miles*, et al. (US Patent No. 6,665,495 B1).

Regarding claim 19, *Uzun* discloses:

a. A line card interface (Fig. 4, Element 450) device for carrying traffic having a statistical distribution which varies at a given variation rate, the interface device comprising a selector (Fig. 8, Element 410) and a control device, the selector having plural interface inputs (Fig. 8, Element 440) for connection to a first multi-path connection (Fig. 8, Element 440) plural interface outputs (Fig. 8, Element 460) for connection to a second multi-path connection, (Fig. 8, Element 460) and plural paths connecting the interface inputs to the interface outputs, (Fig. 8 , Element 430) wherein the paths allow transfer of more packets per unit time than are incident per unit time at the plural interface inputs, thereby providing speed-up (Column 32, Lines 36-39). (The system of *Uzun* discloses a switch that utilizes multiple input line card interfaces connected to multiple output line card interfaces sectors via several parallel interfaces and links and a central switch fabric [Fig. 8 and Column 12, Lines 44-64]. The line card interfaces each contain multiple virtual output queues into which the data received from each input in the sector is placed [Fig. 4 and Column 12, Lines 44-64]. Each input card interface has a selector that controls the connection of each VOQ to one of the multiple optical paths [Column 12, Line 65 to Column 13, Line 50]. Likewise each output line card interface receives multiple output paths that have been switched over the switch fabric and controls the

connection of each Output Queue to connect it to the appropriate multi-path optical connection. [Column 13, Lines 50-65]. Finally, the system of *Uzun* provides for a speedup by increasing the number of multi-path connections such that the aggregate rate exceeds the aggregate rate of the input ports [Column 32, Lines 36-39].)

b. The selector further having a core switch to switch the multipath connections (Fig. 4, Element 430).

c. The control device having means for applying control signals to the switch control inputs at a rate corresponding to the rate of statistical variation in input traffic distribution (Column 14, Line 57 to Column 15, Line 5). (The system of *Uzun* implements Round Robin connection of each Virtual Output Group. This results in the cyclic connection of each VOQ to the corresponding Output Shared block. The round robin scheduling is capable of altering the cyclic pattern to allow an Output Group to Transmit Twice if another output group is idle [Column 14, Line 57 to Column 15, Line 5]. Round robin Scheduling can be applied on a Per Group VOQ basis or a per output VOQ basis, depending on the type of Output queuing in use [Column 14, Line 5 to Column 15, Line 5].)

Uzun fails to disclose a line card interface device for carrying traffic having a statistical distribution which varies at a given variation rate, the interface device comprising an optical selector and a control device, the optical selector having plural interface inputs for connection to a first multi-path optical connection, plural interface outputs for connection to a second multi-

path optical connection, and plural optical paths connecting the interface inputs to the interface outputs, wherein the optical paths allow transfer of more packets per unit time than are incident per unit time at the plural interface inputs, thereby providing speed-up, the optical selector further having plural optical switches, each said optical switch being operable to enable passage of optical data therethrough and to prevent passage of optical data therethrough according to control signals, the speed of response to the control signals being substantially less than said line rate, and the control device having means for applying control signals to the switch control inputs at a rate corresponding to the rate of statistical variation in input traffic distribution. In the same field of endeavor, *Miles* discloses a line card interface device for carrying traffic having a statistical distribution which varies at a given variation rate, the interface device comprising an optical selector and a control device, the optical selector having plural interface inputs for connection to a first multi-path optical connection, plural interface outputs for connection to a second multi-path optical connection, and plural optical paths connecting the interface inputs to the interface outputs, wherein the optical paths allow transfer of more packets per unit time than are incident per unit time at the plural interface inputs, thereby providing speed-up, the optical selector further having plural optical switches, each said optical switch being operable to enable passage of optical data therethrough and to prevent passage of optical data therethrough according to control signals, the speed of response to the control signals being substantially less than said line rate, and the control device having means for applying control signals to the switch control inputs at a rate corresponding to the rate of statistical variation in input traffic distribution (Fig. 4 and 6). (The system of *Miles* discloses a cores switch that is comprised of a plurality of optical switches. The switch operates by closing all paths for a particular link except one, the desired output link [Fig. 6 and Column 9, Lines 34-57]. *Miles* further discloses the use of fiber optic transmitters to transmit data between two points.)

Therefore, since *Miles* discloses the use of an optical crossbar switch and optical connections, it would have been obvious to implement the optical crossbar and transmission of *Miles* into the teachings of *Uzun* by utilizing optical components to implement the connections of *Uzun* by implementing a separate optical crossbar link for each multipath optical connection and implementing the multipath optical connections between the core switch and the ingress and egress line cards using optical transmission, as taught by *Miles*. The motive to combine is to allow the use of optical transmission, thereby increasing bandwidth.

Regarding claim 20, *Uzun* discloses a line card interface wherein the paths are spatially distinct and are greater in number than the number of the plural interface inputs to provide spatial speed-up (Column 32, Lines 36-39). (The system of *Uzun* provides for a speedup by increasing the number of multi-path optical connections such that the aggregate rate exceeds the aggregate rate of the input ports [Column 32, Lines 36-39].)

Uzun fails to disclose a line card interface wherein the optical paths are spatially distinct and are greater in number than the number of the plural interface inputs to provide spatial speed-up. In the same field of endeavor, *Miles* discloses a line card interface wherein the optical paths are spatially distinct and are greater in number than the number of the plural interface inputs to provide spatial speed-up (Fig. 4 and 6). (The system of *Miles* discloses a cores switch that is comprised of a plurality of optical switches. The switch operates by closing all paths for a particular link except one, the desired output link [Fig. 6 and Column 9, Lines 34-57]. *Miles* further discloses the use of fiber optic transmitters to transmit data between two points.)

Therefore, since *Miles* discloses the use of an optical crossbar switch and optical connections, it would have been obvious to implement the optical crossbar and transmission of *Miles* into the teachings of *Uzun* by utilizing optical components to implement the speed up connections of *Uzun* by implementing a separate optical crossbar link for each multipath optical

connection and implementing the multipath optical connections between the core switch and the ingress and egress line cards using optical transmission, as taught by *Miles*. The motive to combine is to allow the use of optical transmission, thereby increasing bandwidth.

Regarding claim 21, *Uzun* discloses a line card interface according wherein the interface inputs and outputs are divided into input groups and output groups, each input group having a distributor, said distributor having one or more of said interface inputs and plural outputs, each output group having a multiplexer having an input, one or more interface outputs, (Column 12, Line 65 to Column 13, Line 50) and the paths comprise a connection wherein each input group is connectable to each output group (Column 13, Lines 50-65). (The system of *Uzun* discloses a line card interface wherein each virtual output queue forms an output group [Fig. 45, Element 412 and Column 12, Line 65 to Column 13, Line 50]. Each output group/VOQ is then distributed to the central switch fabric by a multiplexer, which takes each of the VOQs as an input and outputs each to one of its plural line outputs [Fig. 5, Elements jM to jM+M-1] at the appropriate time [Column 12, Line 65 to Column 13, Line 50]. Likewise, the input line card interfaces receive as an input the output from each of the multi-path connections, queues the results, and distributes the transmission of the queues over multiple switch outputs [Fig. 4 and Column 13, Lines 50-65].)

Uzun fails to disclose the use of optical paths to connect devices. In the same field of endeavor, *Miles* discloses the use of optical paths to connect devices (Fig. 4 and 6). (The system of *Miles* discloses a cores switch that is comprised of a plurality of optical switches. The switch operates by closing all paths for a particular link except one, the desired output link [Fig. 6 and Column 9, Lines 34-57]. *Miles* further discloses the use of fiber optic transmitters to transmit data between two points.)

Therefore, since *Miles* discloses the use of an optical crossbar switch and optical connections, it would have been obvious to implement the optical crossbar and transmission of *Miles* into the teachings of *Uzun* by utilizing optical components to implement the connections of *Uzun* by implementing a separate optical crossbar link for each multipath optical connection and implementing the multipath optical connections between the core switch and the ingress and egress line cards using optical transmission, as taught by *Miles*. The motive to combine is to allow the use of optical transmission, thereby increasing bandwidth.

Regarding claim 22, *Uzun* fails to disclose a line card interface according wherein the distributor and the multiplexer are electronic. However, it is officially noted that the use of electric distributors and multiplexers was well known in the art at the time of the invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement electrical distributors and multiplexers into the teachings of *Uzun* by using electronic circuits to perform the distribution and multiplexing functionality.

Regarding claim 23, *Uzun* fails to disclose a line card interface wherein the distributor and the multiplexer are optical. However, it is officially noted that the use of optical distributors and multiplexers was well known in the art at the time of the invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement electrical distributors and multiplexers into the teachings of *Uzun* by using optical circuits to perform the distribution and multiplexing functionality.

Regarding claim 24, *Uzun* discloses a line card interface wherein each input group has a respective input group memory, said distributor having plural outputs for writing to said input group memory and each output group has a respective output group memory, said multiplexer input being connected to receive outputs from said output group memory (Figs. 4 and 5). (The output group of *Uzun* contains multiple VOQs which receive as in input each VOQ and give as

an output one of multiple parallel outputs by the distributor [Fig. 5 and Column 12, Line 65 to Column 13, Line 50]. Likewise, the input line card interfaces form groups that receive as an input the output from each of the multi-path connections, queues the results in memory, and distributes the transmission of the queues over multiple switch outputs [Fig. 4 and Column 13, Lines 50-65].)

Regarding claim 25, *Uzun* fails to disclose a line card interface wherein the optical connection comprises an optical fibre device. In the same field of endeavor, *Miles* discloses a line card interface wherein the optical connection comprises an optical fibre device (Fig. 4 and 6). (The system of *Miles* discloses a cores switch that is comprised of a plurality of optical switches. The switch operates by closing all paths for a particular link except one, the desired output link [Fig. 6 and Column 9, Lines 34-57]. *Miles* further discloses the use of fiber optic transmitters to transmit data between two points.)

Therefore, since *Miles* discloses the use of an optical crossbar switch and optical connections, it would have been obvious to implement the optical crossbar and transmission of *Miles* into the teachings of *Uzun* by utilizing optical components to implement the connections of *Uzun* by implementing a separate optical crossbar link for each multipath optical connection and implementing the multipath optical connections between the core switch and the ingress and egress line cards using optical transmission, as taught by *Miles*. The motive to combine is to allow the use of optical transmission, thereby increasing bandwidth.

Regarding claim 26, *Uzun* fails to disclose a line card interface wherein the optical connection comprises optical components providing free-space paths in use. In the same field of endeavor, *Miles* discloses a line card interface wherein the optical connection comprises optical components providing free-space paths in use (Fig. 4 and 6). (The system of *Miles* discloses a cores switch that is comprised of a plurality of optical switches. The switch operates

by closing all paths for a particular link except one, the desired output link [Fig. 6 and Column 9, Lines 34-57]. *Miles* further discloses the use of fiber optic transmitters to transmit data between two points.)

Therefore, since *Miles* discloses the use of an optical crossbar switch and optical connections, it would have been obvious to implement the optical crossbar and transmission of *Miles* into the teachings of *Uzun* by utilizing optical components to implement the connections of *Uzun* by implementing a separate optical crossbar link for each multipath optical connection and implementing the multipath optical connections between the core switch and the ingress and egress line cards using optical transmission, as taught by *Miles*. The motive to combine is to allow the use of optical transmission, thereby increasing bandwidth.

Regarding claim 27, *Uzun* discloses a line card interface wherein each input group has the same number of inputs as the number of outputs of said output groups (Fig. 5, VOQ). (The system of *Uzun* may comprise one VOQ for each output port [Fig. 5, VOQ].)

Regarding claim 29, *Uzun* fails to disclose a line card interface having latching circuitry for storing packet data for input to said interface inputs whereby said multi-path optical connections have a line rate reduced compared to said line rate. In the same field of endeavor, *Miles* discloses a line card interface having latching circuitry for storing packet data for input to said interface inputs whereby said multi-path optical connections have a line rate reduced compared to said line rate (Figs 21 and Fig. 13, Element 138). (The system of *Miles* discloses that the core switch module transmits and receives data via multiple parallel streams destined for the same output transmitted simultaneously via dense wavelength division multiplexing [Figs. 14 and 15 and Column 21, Lines 36-60]. The system further discloses that in one embodiment, a petabit router is constructed [Figs. 19, 20 and 21]. In this embodiment, multiple parallel transmission paths are used to satisfy the bandwidth requirements of the system, transmitting

multiple bundles of multiple sets of DWDM multiplexed data transmitted at 40Gbps for each channel [Column 26, Lines 16-46]. The input bandwidth of a port in this embodiment is 16 Terabit/13 Input Ports [See Fig. 20]. Therefore, each 40Gbps channel is significantly smaller then the input bandwidth. Finally, it is inherent that the system of *Miles* has latching circuitry in the receiving DWDM de-multiplexer, as the signal could not be received without synchronizing the receiver.)

Therefore, since *Miles* discloses decomposing a high speed input port into multiple DWDM multiplexed signals at the core router, it would have been obvious to a person of ordinary skill to implement the DWDM de-multiplexing and of *Miles* into the teachings of *Uzun* by de-composing each of the links to the core switch module into multiple parallel DWDM low speed links and transmitting the parallel low speed links in parallel across the core switch. The motive to combine is to reduce hardware costs and memory bandwidth requirements by using lower speed links in parallel.

13. **Claim 28** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) and *Miles*, et al. (US Patent No. 6,665,495 B1) as applied to claim 21 and further in view of *Carvey*, et al. (US Patent No. 6,934,471 B1).

Regarding claim 28, *Uzun* fails to disclose a line card interface wherein each memory is a dual-port memory having an input port for writing to the memory and an output port for reading from the memory. In the same field of endeavor, *Carvey* discloses a line card interface wherein each memory is a dual-port memory having an input port for writing to the memory and an output port for reading from the memory (Column 4, Lines 43-56). (The system of *Carvey*

discloses the use of dual ported memory to enable simultaneous writing and reading to the same memory unit.)

Therefore, since *Carvey* discloses the use of dual ported memory, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the dual ported memory of *Carvey* into the teachings of *Uzun* by implementing dual ported memory for the buffers of *Uzun*. The motive to combine is to increase speed by allowing simultaneous write and read access to memory.

14. **Claim 30** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) in view of *Horlin*, et al. (Us Patent No. 6,993,018).

Regarding claim 30, *Uzun* discloses:

a. A device for providing balanced packet traffic at a set of nodes, the device having a first plurality of input ports (Fig. 4, Element 450) and a first plurality of output ports, (Fig. 4, Element 470) packet traffic being incident at said input ports.

b. The device comprising a first-third stages in series (Fig. 4, Elements 410 and 420), the first and third stages each having said plurality of deserialisers (Fig. 5, IVOQs), said plurality of multiplexers, (Fig. 5, Elements jM to jM+M-1) and a fixed transpose connection (Fig. 4, Element 430). (The system of *Uzun* discloses a first stage sub-module wherein each virtual output queue forms an output group [Fig. 45, Element 412 and Column 12, Line 65 to Column 13, Line 50]. Each output group/VOQ is then distributed to the second stage by a multiplexer for that first stage sub-unit, which takes

each of the VOQs as an input and outputs each to one of its plural line outputs [Fig. 5, Elements jM to jM+M-1] at the appropriate time [Column 12, Line 65 to Column 13, Line 50]. Likewise, the third stage sub-modules receive as an input the output from each of the multi-path connections, queues the results, and distribute the transmission of the queues over multiple switch outputs [Fig. 4 and Column 13, Lines 50-65].)

c. Each deserialiser having at least one input and said plurality of outputs, said at least one input forming a respective one of said input ports, each multiplexer having said plurality of inputs and at least one output, said at least one output forming a respective one of said output ports (Fig. 4, Elements 422 and 470 - See (a), Supra).

d. Each fixed transpose connection connecting respective outputs of each deserialiser to a respective input of each multiplexer (Fig. 4, element 430 – See (a), Supra).

Uzun fails to disclose the second stage having said plurality of sets of packet data queues, each set of packet data queues comprising said plurality of queues, each set being disposed to receive data from a respective multiplexer of the first stage and to furnish data to a respective deserialiser of the third stage. In the same field of endeavor, *Horlin* disclose the second stage having said plurality of sets of packet data queues, each set of packet data queues comprising said plurality of queues, each set being disposed to receive data from a respective multiplexer of the first stage and to furnish data to a respective deserialiser of the third stage (Fig. 1). (The system of *Horlin* discloses a core switch that contains a buffer for each input and output port combination.)

Therefore, since *Horlin* discloses the use of an output buffered core module, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the output buffers of *Horlin* into the teaching of *Uzun* by implementing the core switch using a buffered core switch. The motive to combine is to buffer data at the core, thereby reducing the blocking probability of the switch.

15. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Uzun*, et al. (US Patent No. 6,961,342 B1) as applied to claim 31 and further in view of *Miles*, et al. (US Patent No. 6,665,495 B1).

Regarding claim 32, *Uzun* fails to disclose a method wherein the method includes latching packet data prior to said transposing step interface inputs whereby optical connections in said transposing steps have a line rate reduced compared to an external line rate. In the same field of endeavor, *Miles* discloses a method wherein the method includes latching packet data prior to said transposing step interface inputs whereby optical connections in said transposing steps have a line rate reduced compared to an external line rate (Figs 21 and Fig. 13, Element 138). (The system of *Miles* discloses that the core switch module transmits and receives data via multiple parallel streams destined for the same output transmitted simultaneously via dense wavelength division multiplexing [Figs. 14 and 15 and Column 21, Lines 36-60]. The system further discloses that in one embodiment, a petabit router is constructed [Figs. 19, 20 and 21]. In this embodiment, multiple parallel transmission paths are used to satisfy the bandwidth requirements of the system, transmitting multiple bundles of multiple sets of DWDM multiplexed data transmitted at 40Gbps for each channel [Column 26, Lines 16-46]. The input bandwidth of a port in this embodiment is 16 Terabit/13 Input Ports [See

Fig. 20]. Therefore, each 40Gbps channel is significantly smaller then the input bandwidth. Finally, it is inherent that the system of *Miles* has latching circuitry in the receiving DWDM de-multiplexer, as the signal could not be received without synchronizing the receiver.)

Therefore, since *Miles* discloses decomposing a high speed input port into multiple DWDM multiplexed signals at the core router, it would have been obvious to a person of ordinary skill to implement the DWDM de-multiplexing and of *Miles* into the teachings of *Uzun* by de-composing each of the links to the core switch module into multiple parallel DWDM low speed links and transmitting the parallel low speed links in parallel across the core switch. The motive to combine is to reduce hardware costs and memory bandwidth requirements by using lower speed links in parallel.

Response to Arguments

16. Applicant's arguments, see applicant's response to election/restriction, filed 23 October 2008, with respect to the restriction of claims 1-34 have been fully considered and are persuasive. The grounds of restriction has been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Crutchfield whose telephone number is (571) 270-3989. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel Ryman can be reached on (571) 272-3152. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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3/2/2009

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